



ZYNQ US+ RFSOC DIGITAL RF TRANSCEIVER

A 3U VPX multi - channel RF processor based on the Xilinx XQ-ZU28DR RF System on Chip (RFSoc). Offering 8 ADC and 8 DAC channels in a radiation-mitigated design, the RF processor includes on-board DDR4, NAND and redundant NOR memory, as well as a high-speed mezzanine site. Mezzanine site supports RF-differential pairs, synchronous control interface and high-speed GPIO for a wide variety of RF Front Ends and applications.



8 Simultaneous wideband
TX and RX Channels with
on-board processing

Multi-Channel RF and Processing

Trident's RDRT is based on our powerful, flexible multifunction RF and processing architecture, providing programmability over all key RF/Processing features in a very small size, weight, and power footprint. A mission enabling design, the RDRT can be incorporated at the module level or used as part of Trident's MFREU Products.

Mission Ready

A proven Radiation Effects Mitigated architecture, coupled with radiation tolerant components, redundancy and a robust mechanical design, provide a low C-SWaP, high reliability module for a wide range of applications. Hardware, Software, Firmware customization available with a wide range of FW/SW deployment options.

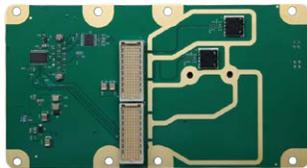
RFSoc Digital RF Transceiver (RDRT)

Mezzanine Options

Multi- Channel Wideband

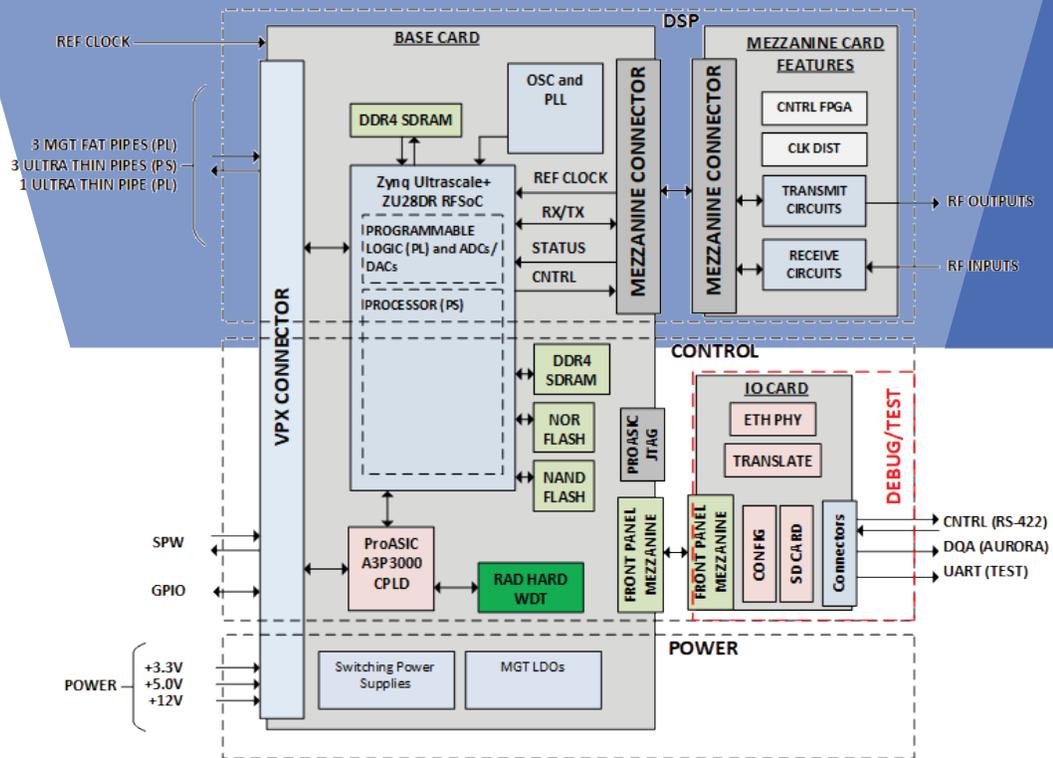


RF Front End Conditioning



Custom - Contact Us

Active and Passive RF Front Ends
High-Speed GPIO and Control
Custom Device Integration



Specifications

SWaP
RFSoc
Memory

Mezzanine Site

Fault Tolerance

Reliability

RF Performance

3U VPX, 1" pitch, < 900g, ~24 W (TYP), +65 C rail temp
Xilinx Zynq UltraScale+ RFSoc XQZU28DR-1FFRC1760M
4 GB PL and 4 GB PS high-speed DDR4; 50 Gbit/sec sustained read/write with ECC
1 GB NAND Flash
128 MB Redundant NOR Flash
8-pairs (4 TX and 4 RX) 100-ohm differential RF
Configurable, high-speed GPIO
Configuration Upset Immune ProASIC for RFSoc Power Control
RHBD Watchdog Timer
TID: 25 kRad component level / 100 kRad unit level (TYP)
No DESL LET ≤ 37 MeV-cm²/mg
Eight 12-bit 4 GSPs ADCs
Eight 14-bit 6.5 GSPs DACs

ZU48DR Gen3 Upgrade Planned

RDRT Features

Ruggedization
Application Processing Unit
Real-Time Processing Unit
Connectivity
Programmable Logic (PL)

XQ-package in LVAUX SEL-mitigated Configuration
Quad-Core ARM Cortex-A53
Dual-core ARM Cortex-R5F
4 PS-GTR, 16 GTY Transceivers
850,560 Flip-Flops, 425,280 LUTs, 1,080 Block RAM, 4,272 DSP Slices

RDRT Development Kits Available

Contact Us: SES-BD@tridsys.com