SQDRT

SPACE QUALIFIED DIGITAL RF TRANSCEIVER

A high, performance, high-reliability 3U VPX RF processor based on the Xilinx Virtex-5QV FPGA with a high-speed ADC/DAC/PLL Mezzanine Card. Multiple build options to support orbital and interplanetary missions including Synthetic Aperture Radar, Communications, Signal Collection/Analysis, On-Board Processing and more. On-orbit since 2019.

Mission Ready Multi-Function RF and On-Board Processing

Re-programmable Multi-Function RF

Trident's SQDRT is based on our powerful, flexible multifunction RF and processing architecture, providing programmability over all key RF/Processing features in a very small size, weight, and power footprint. A mission enabling design, the SQDRT can be incorporated at the module level or used as part of Trident's MFREU Products.

Mission Ready

TRL9 with multiple RF modalities, a mission-ready solution using radiation-hardened parts, redundancy, a robust mechanical design and multiple build options to provide a low C-SWaP, high performance module. Reference designs and custom FW development available as well as custom integration for a wide range of missions.

TRIDENT
LIGHTRIDGE SOLUTIONS

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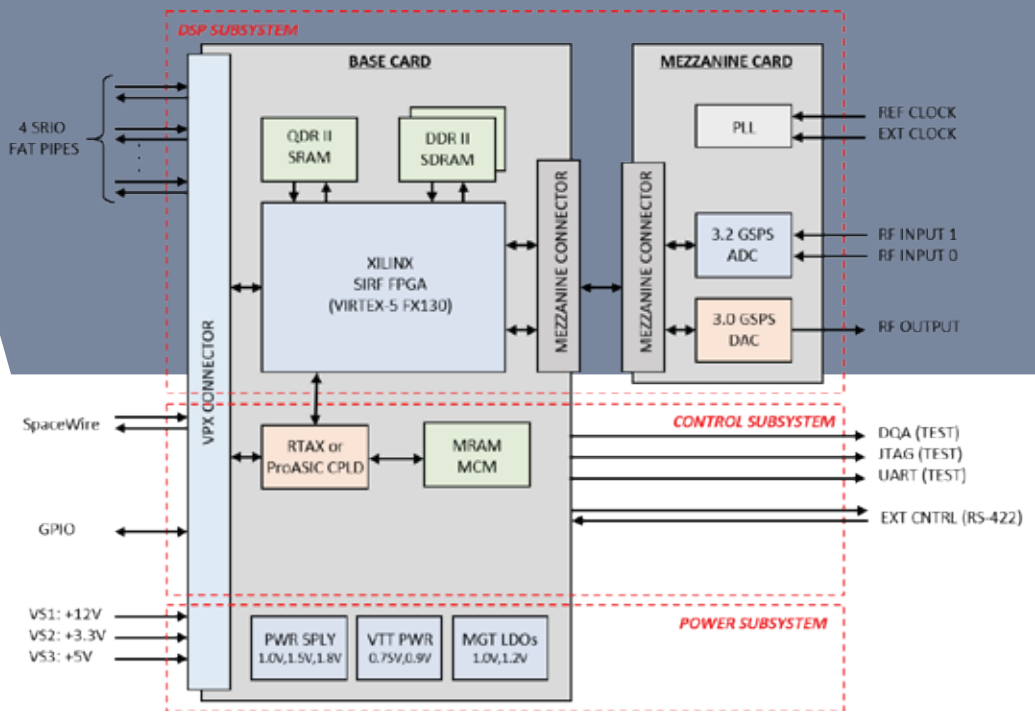
Space Qualified Digital RF Transceiver



Mezzanine Options

Wideband Receiver & Exciter
Dual 12-bit ADC - ADC12D1600QML
Single 12-bit DAC - EV12DS130B
1.6 GHz On-Board Q-Tech Oscillator

8-Channel Sampler
Eight, 12-bit/50 MSps ADCs - RHF1201
Channel synchronization
CAL-tone distribution network

Specifications

SWaP	3U VPX, 1" pitch, < 800g (mezzanine dependent), <50 W (FPGA and Mezzanine) -20 C to +50 C operating temperature range Accepts VITA-78 +12V, +3.3V, +5V Power Rails
FPGA Options	Xilinx Virtex5 XQR5VFX130 or XQ5VFX130T depending on build option
Memory	16 MB QDR II+ SRAM Memory w/EDAC (2M x 72-bit) 1024 MB DDR II SDRAM memory w/EDAC (two independent 64M x 72-bit banks) MRAM for FPGA Configuration and Load Storage
Mezzanine Site	High-speed LVDS and GPIO interface Coherent Exciter/Receiver (12-bit 3.0 GSPS DAC and 12-bit 3.2 GSPS ADC) On-board PLL/oscillator or from external reference clock (up to 2 GHz)
Reliability	Balanced design assurance plan for Class A-D Missions Fault-tolerant Microsemi CPLD to configure FPGA and low-level board monitor/control All components selected for high latch up immunity and total dose, up to 100 krad Radiation-hardened POL voltage-converters for on-board power generation

Additional Features

Ruggedization	High-Shock, High-Vibration, Up to QML Class
Interfaces	Serial RapidIO, SpaceWire, LVDS, LVTTL and single-ended 50 ohm RF
FPGA	131,072 CLBs, 10,728 Kb Max Block RAM, 320 DSP Slices
Reprogrammability	Up to two (2) simultaneous FPGA bit files in MRAM (compression required)
Customization	Custom FW and custom mezzanine designs available from reference designs

Contact Us: SES-BD@tridsys.com