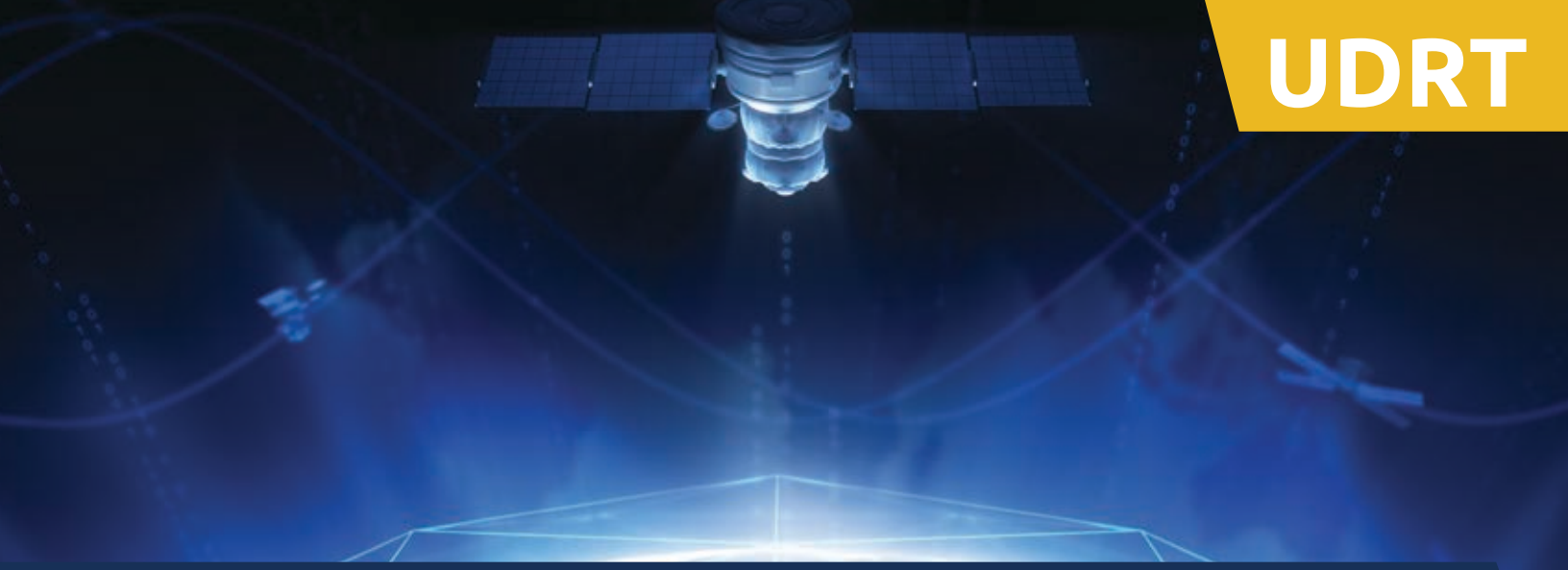

UDRT

ZYNQ ULTRASCALE+ DIGITAL RF TRANSCEIVER

A 3U VPX processor based on the Xilinx XQ-ZU19EG Multi-Processor System on Chip (MPSoC). A radiation-mitigated design, the processor includes on-board DDR4, NAND and redundant NOR memory, as well as a high-speed mezzanine site. Mezzanine cards include a 1 TB SSD or > 3 GSps Dual-ADC/DAC with JES204B clocking; customization available. On-orbit since 2020.

Mission Ready
Multi-Function RF and
On-Board Processing

On-Orbit Processing and RF

Trident's UDRT is based on our powerful, flexible multifunction RF and processing architecture, providing programmability over all key RF/Processing features in a very small size, weight, and power footprint. A mission enabling design, the UDRT can be incorporated at the module level or used as part of Trident's MFREU Products.

Mission Ready

TRL9 on several LEO missions (GEO 2022), a proven Radiation Effects Mitigated architecture, coupled with radiation tolerant components, redundancy and a robust mechanical design, provide a low C-SWaP, high reliability module for a wide range of applications. Hardware, Software, Firmware customization available with a wide range of FW/SW deployment options.

TRIDENT
LIGHTRIDGE SOLUTIONS

www.tridsys.com
703-273-1012

10201 Fairfax Blvd, Suite 300
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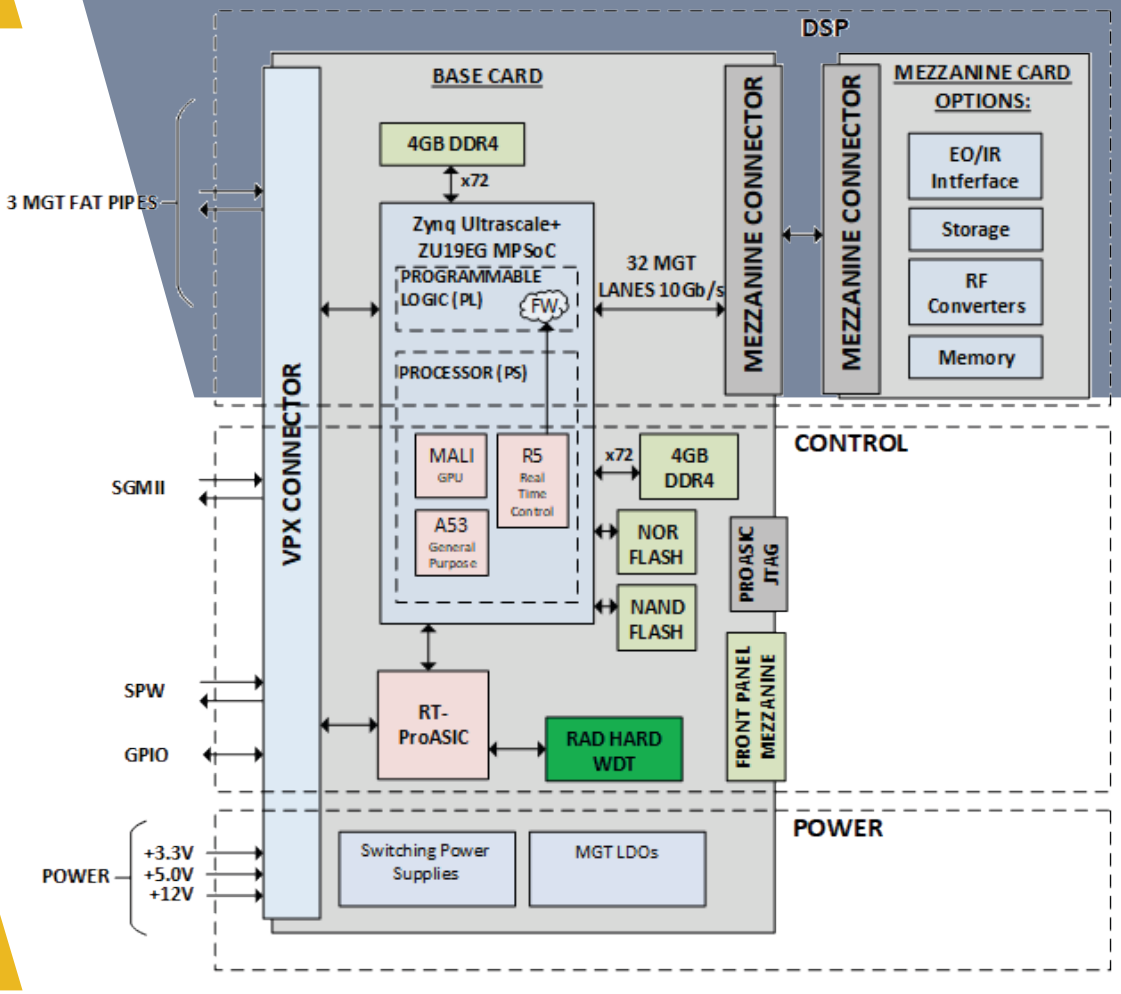
ZYNQ UltraScale+ Digital RF Transceiver

Mezzanine Options

ADC/DAC/PLL

SSD Storage

Custom - Contact Us



Specifications

SWaP	3U VPX, 1" pitch, < 900g, ~24 W (TYP), +65 C rail temp
MPSoC	Xilinx Zynq UltraScale+ XQZU19EG-1FFRC1760M
Memory	4 GB PL and 4 GB PS high-speed DDR4; 50 Gbit/sec sustained read/write with ECC
	1 GB NAND Flash
	128 MB Redundant NOR Flash
Mezzanine Site	8-bands of GTH Transceivers; 10 Gb/sec Lanes
	ADC/DAC/PLL, SSD, and Custom Mezzanine Cards Available
Fault Tolerance	Configuration Upset Immune ProASIC for MPSoC Power Control
	RHBD Watchdog Timer
Reliability	TID: 25 kRad component level / 100 kRad unit level (TYP)
	SEE Mitigated Design Validated Under Test
	No DSEL: LET <= 37 MeV-cm^2/mg
	Balanced design assurance plan for Class B-D Missions
	On-Orbit since 2020

Zynq UltraScale+ Features

UDRT DEVELOPMENT KITS AVAILABLE

Ruggedization	XQ-package in LVAUX SEL-mitigated Configuration
Application Processing Unit	Quad-Core ARM CortexTM-A53
Real-Time Processing Unit	Dual-core ARM CortexTM-R5
Graphics Processing Unit	ARM Mali-400MP2
Programmable Logic (PL)	1,045,440 Flip Flops, 522,720 LUTs, 984 Block RAM, 1,968 DSP Slices

Contact Us: SES-BD@tridsys.com