

VDRT

VERSAL DIGITAL RF TRANSCEIVER AVAILABLE Q2 - 2022

The VDRT is a revolutionary 3U VPX processor based on the Xilinx VC1902 Adaptive Compute Acceleration Platform (ACAP) with AI core. The VDRT will provide never-before available processing power and mezzanine expansion in an industry leading C-SWaP product. Modules and development kits available Q2-2022.



Breakthrough
Performance in a
3U VPX Module

RF and Processing On The Edge

Trident's VDRT leverages the full capability of the revolutionary Xilinx Versal ACAP. The VDRT combines Scalar Engines, Adaptable Engines, Intelligent Engines in a fully software programmable platform. Built on Trident's demonstrated 3U VPX architecture, the VDRT will enable a wide range of on-orbit RF and processing previously not available.

Mission Renabling

A proven Radiation Effects Mitigated architecture, coupled with radiation tolerant components, redundancy and a robust mechanical design, provide a low C-SWaP, high reliability module for a wide range of applications. Hardware, Software, Firmware customization available with a wide range of FW/SW deployment options.

UNDER DEVELOPMENT - AVAILABLE Q2 - 2022

TRIDENT

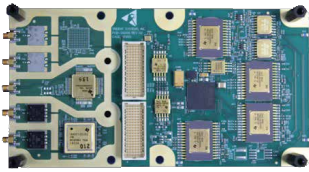
www.tridsys.com
703-273-1012

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Fairfax, VA 22030

Versal Digital RF Transceiver

Mezzanine Options

ADC/DAC/PLL



SSD Storage



Custom - Contact Us

Specifications

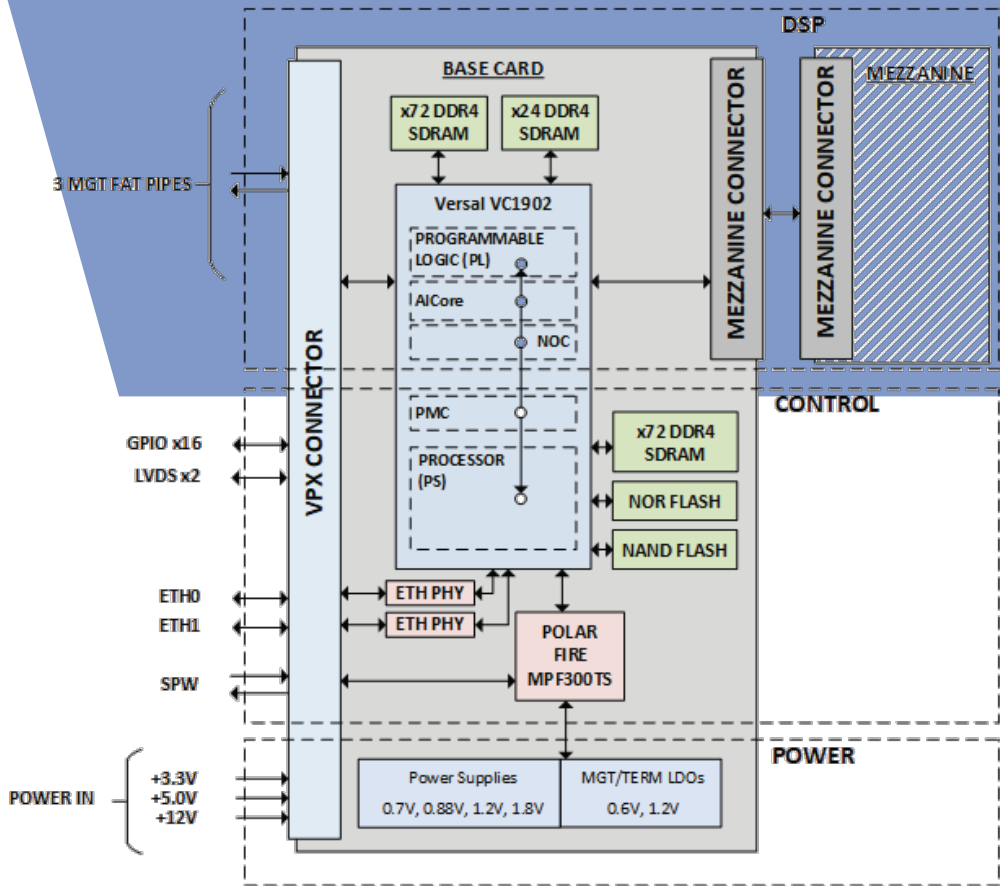
SWaP
Processor

Memory

I/O
Mezzanine Site

Fault Tolerance

Reliability



3U VPX, 1" pitch, < 900g, ~TBD W (TYP), +65 C rail temp
Xilinx Versal AI Core XQ+VC1902

Programmable Network on Chip (NoC)

Two (independent) 8 GB [TBR] x72 DDR4 Memory Banks with ECC

One 1 GB x24 DDR Memory Bank with ECC

DDR4 banks are assignable based on application

1 GB NAND Flash; 128 MB Redundant NOR Flash

PCIe Gen4 compliance; 32.75 Gb/s transceivers

16 GTY transceivers

Compatible with ADC/DAC/PLL, SSD, and Custom Mezzanine Cards

Configuration Upset Immune PolarFire System Controller

RHBD Watchdog Timer

Balanced design assurance plan for Class B-D Missions

VC1902 Features

Ruggedization
Application Processing Unit
Real-Time Processing Unit
AI Core Engines
Programmable Logic (PL)

Lidless XQ+ package [TBR]

Dual-Core ARM Cortex™-A72

Dual-core ARM Cortex™-R5F

400

899,840 LUTs, 191Mb Block RAM, 1,968 DSP Slices

VDRT DEVELOPMENT KITS Q2 - 2022

Contact Us: ES-BD@tridsys.com

TRIDENT

www.tridsys.com
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